1. FIFO control signals includes wr\_clk, rd\_clk, wr\_rst, rd\_rst, and prog\_full. wr\_rst and rd\_rst are reset signals that we use to reset the FIFO buffer before each frame read to make sure the FIFO is empty before start reading. wr\_clk and rd\_clk are used to write into and read from the FIFO. In our case, we connect wr\_clk to FPGA clock and rd\_clk to okClk. Prog\_full signal will notify that there are one block of data in FIFO available to be read. We connect prog\_full to the ep\_ready of the Pipe so the BTPipe know the FIFO is ready and read the next block from it.
2. FIFO overflow can happen when there is a delay between the python code signal the FPGA to read a frame and python start reading from BTPipeOut. In this scenario, the FPGA will read frame data continuously into the FIFO before data start to be read through BTPipeOUT, therefore overflowing the buffer.